REMARKS

Applicant respectfully requests reconsideration of the present application in view of the foregoing amendments and in view of the reasons that follow.

Claims 47, 65, 69, 73 and 77 are currently being amended.

This amendment adds, changes and/or deletes claims in this application. A detailed listing of all claims that are, or were, in the application, irrespective of whether the claims remain under examination in the application, is presented, with an appropriate defined status identifier.

After amending the claims as set forth above, claims 23-30 and 47-78 are now pending in this application.

Drawings

In Section 6 of the Office Action, the Examiner objected the drawings as not showing every feature of the invention specified in the claims. Applicant has added FIG. 9, which was previously enclosed with the RCE/Amendment of July 17, 2003. It appears that the Examiner never received the drawing FIG. 9 in the fax transmission. A copy of the faxed RCE/Amendment transmission of July 17, 2003 is attached herewith, including FIG. 9. Applicant respectfully requests the withdrawal of the drawing objection of Claims 47-78 because the drawing FIG. 9 shows "the substrate of first material and the optical layer forming of the plurality of optical pathways overlaying substrate recited in claims 47-78 in combination with FIG. 8.

In Section 7 of the Office Action, the Examiner objected to the drawings because reference characters "720" and "705" both being used to designate the same element in FIG. 8. Further, the Examiner indicated that the numerical references "730" and "710" designate the same part in FIG. 8. Applicant respectfully submits that the drawings appear to be clear and reference character "720" and "705" are clearly described in the specification. Applicant refers the Examiner to the second paragraph starting on page 10 of the original specification. What is

disclosed is a "substrate 705 (e.g., silicon, gallium arsenide, etc.) may be overlaid with second material "710" (e.g., doped silicon, doped gallium arsenide, other non-doped materials, etc.) forming a plurality of gates patterned in second material "710". Further, the device may include a plurality of laser light sources 720 having a first layer 730 (e.g., semiconductor) overlaid with a second layer 740 (e.g., semiconductor) and having a built junction 750 there between. Accordingly, the arrow tipped lead line associated with 720 is pointing to a laser light source which comprises the three layers 730, 740 and 750, whereas 705 is indicating the substrate along the bottom of the device shown in FIG. 8. Accordingly, Applicant respectfully requests the withdrawal of the objection to character 720 and 705 being used to designate the same elements in FIG. 8. It is clear that the elements to which each referenced number is directed is clear.

The Examiner also objected to the drawings because references 730 and 710 designate the same part in FIG. 8. Applicant respectfully requests that the Examiner withdraw the objection because it is clear from the specification, again in the second paragraph starting on page 10 of the original specification, that there is a patterned gate structure 710 and there is a substrate 705. These two layers are clearly different layers in FIG. 8 and Applicant does not understand how it could be interpreted in any other way. The combination of the specification and FIG. 8 make clear that reference numeral 730 and 710 do not designate the same cart. Accordingly, Applicant respectfully requests the withdrawal of the objection.

Response To Amendment

In Section 8 of the Office Action, the Examiner indicated that the Applicant appears to submit a new Figure, Figure 9, yet no such drawing is submitted. Applicant respectfully submits that Figure 9 was submitted with the RCE/Amendment of July 17, 2003. Applicant has attached evidence of that submission. Accordingly, Applicant requests that the attached Figure 9 be accepted. In Section 10 of the Office Action, the Examiner rejected Claims 47-78 under 35 U.S.C. § 112, first paragraph, because "the specifications and claims fail to teach what is considered to be an 'interference line'." Applicant directs the Examiner's attention to the first full paragraph of page 5 of Applicant's specification which states "light waves in interference

region 25 destructively interfere, in particular, along line 35, which is substantially aligned with output 30." Further, in the first partial paragraph of page 6, Applicant discloses "one of ordinary skill in the art may calculate the location of output 30, such that output 30 is substantially aligned with the interference line such as line 35 (FIG. 2)." Accordingly, Applicant believes that the description of interference line 35 is well provided in the specification. Applicant does not state that there may be more than just one interference line. The Examiner asserts that "it is therefore not possible to have just an interference line and event to determine an interference line." However, Applicant does not claim or disclose that there is just one interference line. In fact, Applicant discloses a plurality of interference lines within the interference region (See e.g., FIGS. 2-5). Accordingly, Applicant requests that the rejections of Claims 47-78 under 35 U.S.C. § 112, be withdrawn.

In Section 11 of the Office Action, the Examiner rejected Claims 68-73, and 77 under 35 U.S.C. § 112, first paragraph thus, failing to comply with the enablement requirement. With regard to Claim 73, the Examiner asserts that Claim 77 fails to teach how could "the interference region is configured to cause cancellation of light exiting the interference output when no light is provided to both of first and second coherent light inputs." Applicant has amended independent Claim 73 to recite "wherein the interference region is configured to cause substantially no light exiting the interference region output when light is provided to the interference region through both the first optical pathway and the second optical pathway, and when no light is provided to both of the first and second optical pathway." Accordingly, Applicant respectfully requests the withdrawal of the rejection of Claim 73 under 35 U.S.C. § 112, as Applicant submits that Claim 73 is enabled, as amended.

With regard to Claims 68 and 77, the Examiner states that "the specifications and the claims also fail to teach how could the optical logic circuit provide both the NOT and (NAND) logical functions, as recited in Claims 68 and 77. Applicant respectfully submits that the construction of a NOT gate and a NOT AND gate is detailed in Applicant's specification. Applicant directs the Examiner's attention to the first full paragraph on page 6 through the end of

page 8. Applicant has described the use of the NAND gates as a "universal" function, that is it can be used, alone or in combination with other NAND gates or logic gates, to construct an AND gate, an OR gate, an inverter (NOT GATE) or any combination of these functions. Accordingly, Applicant respectfully requests the withdrawal of the objection to Claims 68 and 77.

Claim Objections

In Section 12 of the Office Action, the Examiner objected to Claims 47-78 because of informalities. First the Examiner objects to various claims based on the term "interference line and how can such line be defined or even formed." As described above, Applicant respectfully submits that the specification provides a clear definition for an interference line.

The Examiner also objected to the use of the phrase "the at least two input signals" and the phrase "the interference region" recited in Claim 65, being confusing and indefinite for lack of antecedent basis. Applicant has amended Claim 65 and therefore request that the objection be withdrawn.

Further, the Examiner objected to Claim 69 because the phrases "the first optical pathway", "the second optical pathway", and "the third optical pathway" were confusing and indefinite as lacking in proper antecedent basis. Applicant respectfully submits that Claim 69 has been amended and request that the objection be withdrawn.

Further still, the Examiner objected to Claim 73 as the phrase "the first coherent input" and "the second coherent input" were confusing and indefinite because they lack proper antecedent basis. Applicant respectfully submits that Claim 73 has been amended and request the withdrawal of the rejection.

Yet further still, the Examiner objected to Claim "775" as being misnumbered. Applicant has renumbered the claim as 77. And further have amended the dependency to Claim 76 to provide antecedent basis for "the optical processor". Accordingly, Applicant requests that the objection be withdrawn.

Claim Rejections – 35 U.S.C. § 103

In Section 14 of the Office Action, the Examiner rejected Claims 47-58 and 63-78 under 35 U.S.C. § 103(a) as being unpatenable over the patent issued to Usagawa et al. (U.S. Patent No. 5,233,205). The Examiner asserts that Usagawa et al. teaches an optical logic circuit based on quantum well design." Further, the Examiner asserts that "this reference has met all the limitations of the claims with the exception that an interference line is aligned with the output. However, it is not clear what is considered to be the interference line for the reason stated in the rejection above. But it is understandable that the output gate must be arranged so that the resultant output signal, after the interference as a result of the interference, can be propagated out of the interference region. Such features therefore either inherently met or in obvious medication to one skilled in the art to make the optical logic gate more efficient." Applicant respectfully requests that the issue regarding the "interference line" has been addressed and is clearly disclosed in Applicant's specification. Further, Applicant respectfully disagrees with the Examiner regarding the rejection. Usagawa et al. does not teach an "optical logic circuit" (emphasis added). In fact, the Examiner states that what Usagawa et al. teaches is based on quantum well design. That is, the waves used in the circuit taught by Usagawa et al. are quantum waves, that is waves of carriers which are electrons or holes. What is described by and claimed by Applicant is a circuit in which the pathways are optical pathways and the circuit is an optical logic circuit, that is a circuit which uses light and light sensitive devices. Accordingly, the carriers are not electrons and holes forming the waves, rather what is propagated through the pathways is light with the device relying on the wave-like behavior of light causing interference within the interference region, the interference being created along a predicted interference line and therefore providing an output at a known location based on the input. Usagawa et al. teaches only that "the present invention relates to a semiconductor circuit for executing a logic operation by a quite novel mechanism, or more particularly to a quantum wave circuit . . . utilizing the quantum wave interference effect of the carriers, including electrons and holes." Nowhere does Usagawa et al. disclose, teach, or suggest that a circuit should be built as an optical circuit. Nor is there any suggestion or advantages of building an optical logic circuit. All that is taught in

Usagawa et al. is that a circuit may be built using semiconductor materials to produce quantum waves. Accordingly, Applicant respectfully submits that there is no teaching of an optical logic circuit in Usagawa et al. Even when obviousness is based on a single prior art reference, there must be a showing of a suggestion or motivation to modify the teachings of that reference. See B.F. Goodrich Co. v. Aircraft Breaking Sys. Corp., 72 F.3d 1577, 1582, 37 USPQ2d 1314, 1318 (Fed. Cir. 1996). Here, the teachings of Usagawa et al. are for a quantum well design and there has been no showing or suggestion of a suggestion or motivation to modify those teachings to encompass an optical logic circuit as recited in Applicant's claims. Accordingly, Applicant respectfully submits that Claims 47-58, and 63-78 are not obvious over Usagawa et al. and are therefore allowable.

In Section 15 of the Office Action, the Examiner rejected Claims 59-62 under 35 U.S.C. § 103(a) as being unpatenable over the patent issued to Usagawa et al. as applied to Claim 55 above and further in view of the patent issued to Logan et al. (U.S. Patent No. 3,837,728). Applicant respectfully submits that Claims 59-62 depend from Claim 55 and because Applicant believes that Claim 55 is allowable, Applicant also believes that claims 59-62 are similarly allowable.

Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 06-1447. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 06-1447. If any extensions of time are needed for timely acceptance of papers

submitted herewith, Applicant hereby petitions for such extension under 37 C.F.R. § 1.136 and authorizes payment of any such extensions fees to Deposit Account No. 06-1447.

Respectfully submitted,

Date July 14, 2004

By _____

FOLEY & LARDNER LLP
Customer Number: 26371
Telephone: (414) 297-5730
Facsimile: (414) 297-4900

Alistair K. Chan
Attorney for Applicant
Registration No. 44,603

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MILWAUKEE, WISCONSIN 53202-5306
TELEPHONE: 414.271.2400
FACSIMILE: 414.297.4900
WWW.FOLEYLARDNER.COM

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This is regarding Application No. 09/630,883.

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MESSAGE:

This is regarding Application No. 09/630,883.

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Atty. Dkt. No. 025572-0102

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Khosrow Golshan
Title:	METHOD AND APPARATUS FOR OPTICAL PROCESSING
Appl. No.:	09/630,883
Appl. Filing Date:	08/02/2000
Examiner:	Chang, A.
Art Unit:	2872

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REQUEST FOR CONTINUED EXAMINATION (RCE) TRANSMITTAL

Mail Stop RCE
Commissioner for Patents
PO Box 1450
Alexandria, Virginia 22313-1450

Sir:

This is a Request for Continued Examination (RCE) under 37 C.F.R. § 1.114 of the above-identified application. This RCE and the enclosed items listed below are being filed prior to the earliest of: (1) payment of the issue fee (unless a petition under 37 C.F.R. § 1.313 is granted); (2) abandonment of the application; or (3) the filing of a notice of appeal to the U.S. Court of Appeals for the Federal Circuit under 35 U.S.C. §141, or the commencement of a civil action under 35 U.S.C. §145 or §146 (unless the appeal or civil action is terminated).

1. Submission **required** under 37 C.F.R. §1.114: (check items that apply)

a. Previously submitted:

[ ] Please enter and consider the amendment/reply previously filed on ___.

[ ] Please consider the Affidavit(s)/Declaration(s) previously filed on ___ but not considered.

[ ] Please consider the arguments in the Appeal Brief or Reply Brief under 37 C.F.R. § 1.116 previously filed on ___.

[ ] Other ___.

b. Enclosed are:

[X] Amendment/Reply.

[ ] Affidavit(s)/Declaration(s).

[ ] Information Disclosure Statement.

[ ] Form PTO-1449 with copies of ___ listed reference(s).

[ ] Other .

Miscellaneous:

[ ] Suspension of action of the above-identified application is requested under 37 C.F.R. § 1.103(c) for a period of ___ months.

The filing fee is calculated below:

	Claims as Amended		Previously Paid For		Extra Claims Present		Rate		Fee Totals
RCE Fee 1.17(e)							$750.00		$750.00
Total Claims:	32	–	46	=	0	x	$18.00	=	$0.00
Independents:	4	–	4	=	0	x	$84.00	=	$0.00
First presentation of any Multiple Dependent Claims:						+	$280.00	=	$0.00
							CLAIMS FEE TOTAL:	=	$750.00

[X] Applicant hereby petitions for an extension of time under 37 C.F.R. §1.136(a) for the total number of months checked below:

[X]	Extension for response filed within the first month:	$110.00	$110.00
[ ]	Extension for response filed within the second month:	$410.00	$0.00
[ ]	Extension for response filed within the third month:	$930.00	$0.00
[ ]	Extension for response filed within the fourth month:	$1,450.00	$0.00
[ ]	Extension for response filed within the fifth month:	$1,970.00	$0.00
		EXTENSION FEE TOTAL:	$110.00
		CLAIMS AND EXTENSION FEE TOTAL:	$860.00
[ ]		Small Entity Fees Apply (subtract ½ of above):	$0.00
[ ]		Suspension of action requested under 37 C.F.R. § 1.103(c)	$0.00
		TOTAL FEE:	$860.00

[X] Please charge Deposit Account No. 06-1447 in the amount of $860.00. A duplicate copy of this transmittal is enclosed.

[ ] A check in the amount of $860.00 to cover the filing fee is enclosed.

[X] The Commissioner is hereby authorized to charge any additional fees which may be required regarding this application under 37 C.F.R. §§ 1.16-1.17, or credit any overpayment, to Deposit Account No. 06-1447. Should no proper payment be enclosed herewith, as by a check being in the wrong amount, unsigned, post-dated, otherwise improper or informal or even entirely missing, the Commissioner is authorized to charge the unpaid amount to Deposit Account No. 06-1447.

Please direct all correspondence to the undersigned attorney or agent at the address indicated below.

Respectfully submitted,

Date July 17, 2003

By _____

Alistair K. Chan
Attorney for Applicant
Registration No. 44,603

FOLEY & LARDNER
Suite 3800
777 East Wisconsin Avenue
Milwaukee, Wisconsin 53202-5306
Telephone: (414) 297-5730
Facsimile: (414) 297-4900

Atty. Dkt. No. 025572-0102

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Khosrow Golshan

Title: METHOD AND APPARATUS FOR OPTICAL PROCESSING

Appl. No.: 09/630,883

Filing Date: 08/02/2000

Examiner: Chang, A.

Art Unit: 2872

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AMENDMENT

Mail Stop RCE
Commissioner for Patents
PO Box 1450
Alexandria, Virginia 22313-1450

Sir:

This communication is responsive to the Final Office Action dated March 17, 2003, concerning the above-referenced patent application.

The amendments presented below are in compliance with the revised amendment format permitted in the Notice from the Office of Patent Legal Administration of the U.S. Patent and Trademark Office dated February 10, 2003, and published at 1267 OG 106 on February 25, 2003. Thus, the provisions of 37 CFR 1.121(a), (b), (c) and (d) are waived for amendments made in this application to the claims, specification, and drawings.

Amendments to the Specification begin on page 3 of this document.

Amendments to the Drawings begin on page 5 of this document.

Amendments to the Claims are reflected in the listing of claims which begins on page 6 of this document.

Remarks/Arguments begin on page 12 of this document.

Amendments to the Specification

Please amend the specification as follows:

On page 4, please replace the paragraph beginning at line 7 with the following revised paragraph:

FIG. 7 is an illustrative representation of the cancellation of light due to constructive interference of wavefronts; ~~and~~

On page 4, please replace the paragraph beginning at line 9 with the following revised paragraph:

FIG. 8 is an illustrative representation of a cross section of an optical processing device~~.~~; and

On page 4 after line 10, please add the following new paragraph:

--FIG. 9 is an illustrative representation of the optical NOT gate of FIG. 2 formed on a substrate as depicted in FIG. 8.--

On page 5, please replace the paragraph beginning at line 3 with the following revised paragraph:

As depicted in FIG. 2 and FIG. 9, light may be provided to input 20 simultaneous with the bias light provided to bias input 15. Light from bias input 15 and input 20 are received in interference region 25. Light waves in interference region 25 destructively interfere, in particular, along line 35 which is substantially aligned with output 30. Therefore, output 30 provides a substantially dark output, in other words, the energy of the light coming from interference region 25 is low, i.e., below a predetermined threshold.

On pages 10-11, please replace the paragraph beginning at line 25 with the following revised paragraph:

Therefore, it is possible to construct an optical processing device having a plurality of light sources, such as lasers 600. Further, a plurality of optical gates, forming an optical processor 700, may be formed on a substrate 705, as depicted in FIG. 8 and FIG. 9. Substrate 705 (e.g., silicon, gallium arsenide, etc.) may be overlaid with a second material 710 (e.g., doped silicon, doped gallium arsenide, other nondoped materials, etc.) forming a plurality of gates patterned in second material 710. Further, the device may include a plurality of laser light sources 720 having a first layer 730 (e.g., semiconductor) overlaid with a second layer 740 (e.g., semiconductor) and having a doped junction 750 therebetween. In an exemplary embodiment, optical processor 700 may include a non-translucent layer 760 overlaying substrate 705 and patterned gate structures 710 and semiconductor laser 720, and any other devices formed on substrate 705.

Amendments to the Drawings

Please add the attached 1 sheet (Fig. 9) of informal drawings.

Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Please cancel claims 1-22 and 31-46 without prejudice. Please add new claims 47-78.

Listing of Claims:

Claims 1-22 (Cancelled).

Claims 23-30 (Withdrawn).

Claims 31-46 (Cancelled).

47. (New) An optical logic circuit, comprising:

a substrate comprising a first material;

an optical layer overlaying the substrate the optical layer comprising a second material, the optical layer configured to provide a plurality of optical pathways, the optical pathways forming a plurality of optical logic gates, at least some of the optical logic gates having a first input that receives a constant coherent light input from a light source, a second input that receives a coherent light input which can be selectively turned on and off, an interference region coupled to the first and second light inputs, and an output coupled to the interference region opposite the first and second light inputs;

the interference region comprises the second material, the first and second optical inputs are spaced apart and the output is positioned such that an interference line is aligned with the output,

wherein the optical output signal is a Boolean logic output signal based on the second optical input signal and the optical output signal exits the interference region output.

48. (New) The optical logic circuit of claim 47, wherein the interference region is configured to cause substantial cancellation of light exiting the interference region through the output when the coherent light input to the second input is turned on.

49. (New) The optical logic circuit of claim 47, wherein the interference region includes a third optical input receiving a coherent light input signal which can be selectively turned on and off.

50. (New) The optical logic circuit of claim 49, wherein the interference region is configured to cause substantial cancellation of light exiting the output when coherent light is provided to the interference region through both the second optical input and the third optical input.

51. (New) The optical logic circuit of claim 47, wherein the Boolean logic output is a NOT (inverter) function.

52. (New) The optical logic circuit of claim 47, wherein the Boolean logic output is a NOT AND (NAND) function.

53. (New) The optical logic circuit of claim 47, having a multiplicity of optical pathways and interference regions configured to function as an optical processor.

54. (New) The optical logic circuit of claim 53, wherein the optical processor comprises NOT (inverter) gates and NOT AND (NAND) gates.

55. (New) An optical logic gate for an optical processor, comprising:

a substrate configured of a first material;

a patterned optical layer overlaying the substrate, the optical layer comprising a second material, the patterned optical layer comprising a plurality of optical conduits formed of the second material, at least two of the optical conduits are configured to receive optical input signals, each of the optical input signals provide coherent light inputs, at least one of the optical conduits provides optical output signals, and at least one of the at least two optical input signals is a constant coherent light input signal; and

an interference region coupled to at least two of the optical conduits that are configured to receive optical input signals, the interference is caused along a predetermined axis in the interference region, the interference region is coupled to at least one of the optical conduits configured to provide optical output signals, and the optical conduit receiving output signals is positioned such that the predetermined axis is aligned with the optical conduit receiving the output,

wherein the interference region is configured to provide a Boolean logic output signal based on one optical input signal that may selectively be turned on and off.

56. (New) The optical logic gate of claim 55, wherein the optical logic gate provides a Boolean NOT function as output.

57. (New) The optical logic gate of claim 55, further comprising:

at least three optical conduits configured to receive optical inputs.

58. (New) The optical logic gate of claim 57, wherein the optical logic gate provides a Boolean NOT function as output.

59. (New) The optical logic gate of claim 55, wherein the first material comprises silicon (Si).

60. (New) The optical logic gate of claim 55, wherein the second material comprises doped silicon (Si).

61. (New) The optical logic gate of claim 55, wherein the first material comprises Gallium Arsenide (GaAs).

62. (New) The optical logic gate of claim 55, wherein the second material comprises doped Gallium Arsenide (GaAs).

63. (New) The optical logic gate of claim 55, wherein the optical input signal is generated by a Laser diode.

64. (New) The optical logic gate of claim 55, wherein the optical input signal is generated by a semiconductor diode.

65. (New) A method of providing a Boolean logic optical output signal based on at least two optical input signals, comprising:

providing a first constant coherent light input signal to a first optical input such that the input signal is in an always on condition;

providing a plurality of optical pathways formed of optical transmission material patterned on a substrate material;

providing a second coherent light input signal, the second coherent light input signal being a coherent light input that is selectively turned on and off;

providing a distance between the plurality of optical pathways entering the interference region, the interference region enabling interference of the first constant coherent light input signal and the second coherent light input signal when the coherent light input signal is turned on; and

providing an optical output signal, the optical output signal is based on the at least two input signals and is representative of a Boolean logic function.

66. (New) The method of claim 65, wherein the Boolean logic function is a NOT (inverter) gate.

67. (New) The method of claim 65, wherein the Boolean logic function is a NOT AND (NAND) gate.

68. (New) The method of claim 65, wherein the Boolean logic function is configured of NOT (inverter) gates and NOT AND (NAND) gates.

69. (New) An optical logic circuit, comprising:

a substrate comprising a first material;

an optical layer overlaying the substrate partially comprising a second material, the optical layer is patterned to provide a plurality of optical pathways, at least two optical pathways are configured to provide optical input signals, the optical input signals are coherent light inputs, and at least one optical pathway configured to provide an optical output signal; and

an interference region configured to selectively cause interference of wavefronts of light from the optical input signals entering the interference region, the location of an interference line is based on the distance between the first optical pathway and the second optical pathway entering the interference region and the length of the interference region, the third optical pathway is positioned such that the interference line is aligned with the third optical pathway, the interference is produced along the interference line in the interference region,

wherein the interference region is configured to provide a Boolean logic output signal based on the at least two coherent light input signals.

70. (New) The optical logic circuit of claim 69, wherein the interference region receives a first optical input that may be selectively turned on and off and a constant coherent light input.

71. (New) The optical logic circuit of claim 69, wherein the interference region is configured to cause substantial cancellation of light exiting the interference region output when a light signal is provided to the interference region through the coherent light input, the light signal being selected as on.

72. (New) The optical logic circuit of claim 69, wherein the interference region includes a second coherent light input that may be selectively turned on and off.

73. (New) The optical logic circuit of claim 69, wherein the interference region is configured to cause substantial cancellation of light exiting the interference region output when light is provided to the interference region through both the first coherent

light input and the second coherent light input, and when no light is provided to both of the first and second coherent light inputs.

74. (New) The optical logic circuit of claim 69, wherein the Boolean logic output is a NOT (inverter) function.

75. (New) The optical logic circuit of claim 69, wherein the Boolean logic output is a NOT AND (NAND) function.

76. (New) The optical logic circuit of claim 69, having a multiplicity of optical pathways and interference regions configured to function as an optical processor.

775. (New) The optical logic circuit of claim 69, wherein the optical processor is configured of NOT (inverter) gates and NOT AND (NAND) gates.

78. (New) The optical logic circuit of claim 69, wherein the Boolean logic output is an XOR (exclusive OR) function.

REMARKS

Applicant respectfully requests reconsideration of the present application in view of the foregoing amendments and in view of the reasons which follow.

Drawings

FIG. 9 has been added for clarity. FIG. 9 is a depiction of the optical gate of FIG. 2 formed on the substrate of FIG. 8. The combination of FIG. 2 and FIG. 8 has been well described throughout the specification. Accordingly, no new matter is presented.

DETAILED ACTION

Claim Rejections – 35 U.S.C. § 103

In section 8 of the Office action, the Examiner rejected claims 1, 4-10, 11, 13-15, 17-22, 36 and 38-46 under 35 U.S.C. 103(a) as being unpatentable over the patent issued to Utaka et al. in view of the patent issued to Yang.

Also, in section 9 of the Office action, the Examiner rejected claims 31 and 33-35 rejected under 35 U.S.C. 103(a) as being unpatentable over the patent issued to Yang in view of the patent issued to Utaka et al.

Claims 1-22 and claims 31-46 are cancelled without prejudice. New claims 47-78 have been added.

With regard to independent claims, 47, 55, 69, and 69 neither Utaka et al. nor Yang discloses, teaches, suggests, alone or in any proper combination, an optical logic circuit having a substrate and an optical layer overlaying the substrate. The optical layer is formed with a plurality of optical pathways and an interference region. Further, the optical pathways include two optical inputs to the interference region, one optical input providing a constant source of coherent light. The other of the two optical inputs provides a coherent light input which can be selectively turned on and off (conventionally representative of a binary 1 or 0 respectively). The output of the interference region is

positioned such that an interference line is aligned with the output and therefore wavefronts interfering cause a dark output. Output signals are Boolean logic output signals based on the second optical input signal and the optical output signal exits the interference region output. Utaka et al. teaches a system of optical pathways in which light waves are not coherent in paths I and II, rather the phase of light wave P_i is modulated by inputs P_1 and P_2. Yang teaches a mechanical structure having mechanical gates to provide an interference region. However, Yang does not provide that the optical gates are formed over a substrate using an optical layer that overlays the substrate and forms the optical pathways and interference region.

Further, neither Utaka et al. nor Yang teaches, alone or in any proper combination, an optical logic gate for an optical processor that is formed on a substrate and via a patterned optical layer which overlays the substrate. The optical layer includes a plurality of optical conduits formed of the second material where at least two of the optical conduits are configured to receive optical input signals, each of the optical input signals provide coherent light inputs. Again, Utaka et al. does not provide such light inputs to an interference region and Yang does not provide any teaching or suggestion to provide the mechanical gates formed in an optical layer overlaying a substrate.

Accordingly, independent claims 47, 55, 65, and 69 and their dependent claims are not disclosed, taught, or suggested, alone or in any proper combination of Utaka et al. and Yang. Therefore, independent claims 47, 55, 65, and 69 and their respective dependent claims are therefore allowable.

After amending the claims as set forth above, claims 47-78 are now pending in this application.

Applicant believes that the present application is now in condition for allowance. Favorable reconsideration of the application as amended is respectfully requested.

The Examiner is invited to contact the undersigned by telephone if it is felt that a telephone interview would advance the prosecution of the present application.

Respectfully submitted,

Date July 17, 2003

By _____

Alistair K. Chan
Attorney for Applicant
Registration No. 44,603

FOLEY & LARDNER
Suite 3800
777 East Wisconsin Avenue
Milwaukee, Wisconsin 53202-5306
Telephone: (414) 297-5730
Facsimile: (414) 297-4900